Q.P. Code: **16EC5701** **R16**

**Reg. No:** | | | | | | | | | | |

**SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR**

(AUTONOMOUS)

**M.Tech I Year I Semester (R16) Regular & Supplementary Examinations February 2018**

**VLSI TECHNOLOGY**

(Common to ES & VLSI)

Time: **3 hours** Max. Marks: **60**

(Answer all Five Units **5 X 12 =60** Marks)

**UNIT-I**

| | | | |
|---|---|---|---|
| **1** | a. | Explain different steps involved in preparation CMOS using twin tub process. | 7M |
| | b. | Derive the expression for ZPU/ZPD. | 5M |
| | | **OR** | |
| **2** | a. | Explain a Bi-CMOS inverter with appropriate circuit. | 6M |
| | b. | Explain effect of latch-up in CMOS circuits. | 6M |

**UNIT-II**

| | | | |
|---|---|---|---|
| **3** | a. | Explain switch Logic and Alternative Logic. | 7M |
| | b. | Explain clearly the Scalable design rules. | 5M |
| | | **OR** | |
| **4** | a. | Explain how stick diagrams can be used for layout diagrams. | 7M |
| | b. | Discuss about the effects of scaling down the dimensions of MOS circuits and Systems. | 5M |

**UNIT-III**

| | | | |
|---|---|---|---|
| **5** | a. | Draw the layout diagram of three input NAND gate in CMOS. | 6M |
| | b. | With suitable examples explain about network delays combinational logic circuits. | 6M |
| | | **OR** | |
| **6** | a. | Explain the clocking disciplines and power optimization in sequential systems. | 7M |
| | b. | Explain the structure of LSSD with suitable diagram. | 5M |

**UNIT-IV**

| | | | |
|---|---|---|---|
| **7** | | Explain floor planning methods of chip. | 12 M |
| | | **OR** | |
| **8** | a. | Explain power reduction using Architecture driven voltage scaling method. | 7M |
| | b. | Draw and explain the I/O architecture. | 5M |

**UNIT-V**

| | | | |
|---|---|---|---|
| **9** | a. | With an example give the method involved in the chip design. | 7M |
| | b. | Write about test generation pattern. | 5M |
| | | **OR** | |
| **10** | a. | Write about switch level simulation. | 7M |
| | b. | Write short notes on sequential machine optimizations. | 5M |

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